

The SP8715 is a switchable divide by 64/65, 128/129 programmable divider which is guaranteed to operate up to 1100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 3.6mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

**FEATURES**

- Operation to 1100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

**APPLICATIONS**

- Cellular Telephones
- Cordless Telephones
- Mobile Radio

† ESD precautions must be observed

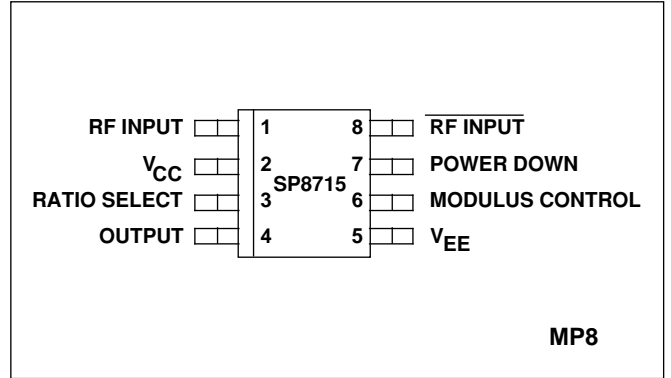


Fig. 1 Pin connections - top view

**ORDERING INFORMATION**

**SP8715 IG MPAS** Industrial Temperature Range  
Miniature Plastic DIL Package

**SP8715 IG MPAC** As above supplied on Tape and Reel

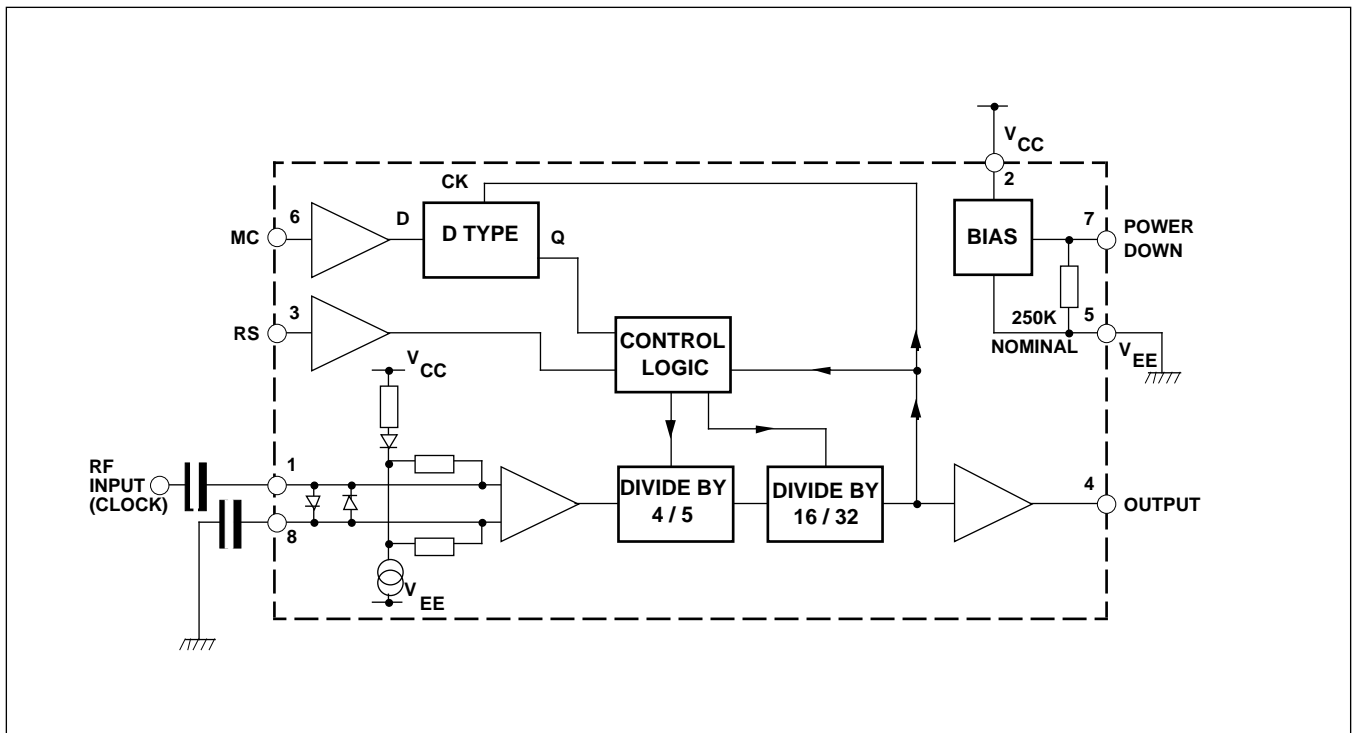


Fig. 2 Block diagram

## SP8715

### ABSOLUTE MAXIMUM RATINGS

Supply voltage ( $V_{EE}=0V$ )	(note 1)	-0.5V to 7V
Control and RF inputs,		
RF output ( $V_{EE}=0V$ )	(note 1)	-0.5V to $V_{CC}+0.5V$
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

### ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

$V_{CC}=+2.7V$  to  $+5.5V$  (with respect to  $V_{EE}$ ), Output load (pin 4) = 10pF,  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$  (note 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current (note 3)		3.6	4.2	mA	Power down input low
Supply current (note 3)		8	50	$\mu A$	Power down input high
Power down high	$V_{CC}-0.5$		$V_{CC}$	V	
Power down low	0		$V_{CC}-2.0$	V	
Modulus control high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 64 or 128
Modulus control low (note 4)	0		$0.4V_{CC}$	V	Divide by 65 or 129
Ratio select high (note 4, 9)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 64 or 65
Ratio select low (note 4, 9)	0		$0.4V_{CC}$	V	Divide by 128 or 129
Max. sinewave input frequency	1100			MHz	See Figure 5
Min. sinewave input frequency			200	MHz	See Figure 5
Min. RF input voltage			50	mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Max. RF input voltage	200			mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Output level (pin 4)	500	600		mV p-p	
Modulus set-up time, $t_s$ (notes 5,6,8)	20			ns	RF input = 1GHz
Modulus hold time, $t_h$ (notes 6,8)			1	ns	RF input = 1GHz
Power down time, $t_{pd}$ (notes 7,8)			10	$\mu s$	See Figure 9
Power down recovery time, $t_{pu}$ (notes 7,8)			6	$\mu s$	See Figure 9

#### NOTES

- All electrical testing is performed at +85°C.
- Typical values are measured at +25°C and  $V_{CC} = +5V$ .
- Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
- Modulus control is latched at the end of the previous cycle.
- See Figure 4.
- See Figure 8.
- These parameters are not tested but are guaranteed by design.
- The ratio select pin is not intended to be switched dynamically.

**OPERATING NOTES**

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors. The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8715 is not suitable for driving TTL or similar devices. The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/ $\mu$ s. POWER DOWN (pin 7) is connected internally to a pull-down resistor. If the battery economy facility is not used, pin 7 should be either left unconnected or connected to  $V_{EE}$ .

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	129
L	H	128
H	L	65
H	H	64

Table 1 Truth table

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Fig. 3 Typical input characteristics

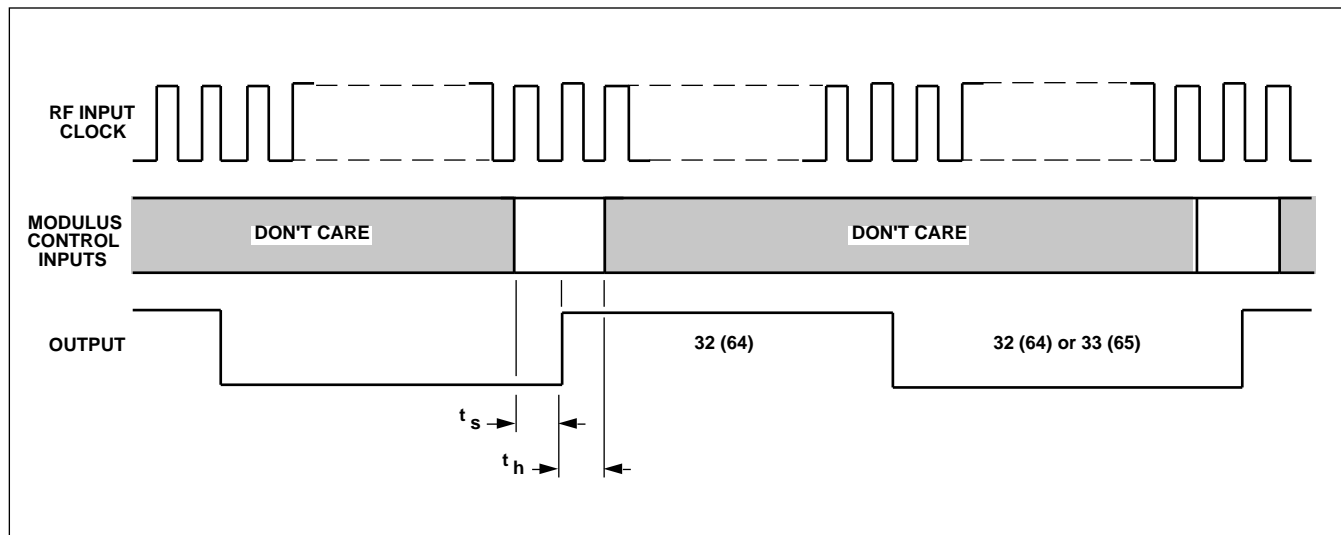


Fig. 4 Modulus control timing diagram

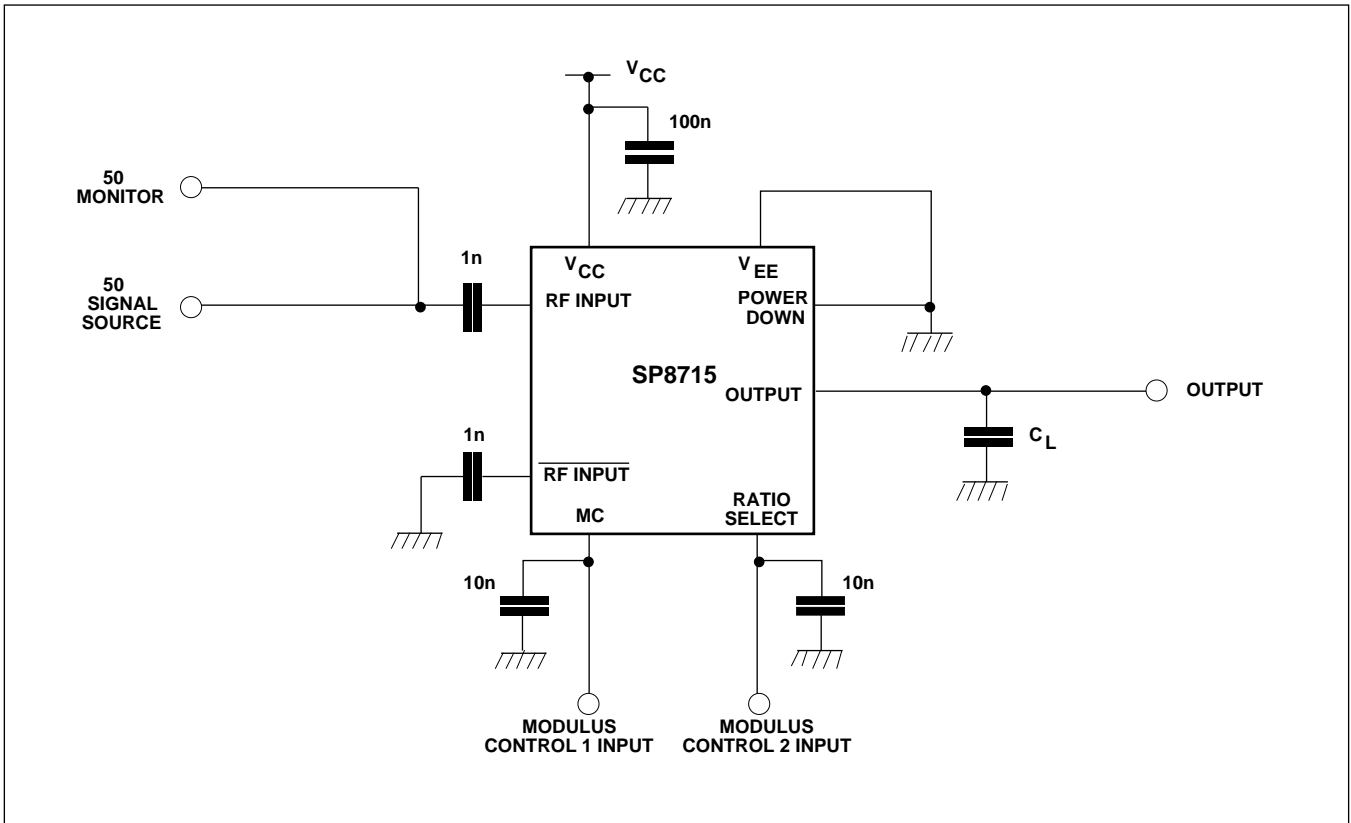


Fig. 5 Toggle frequency test circuit

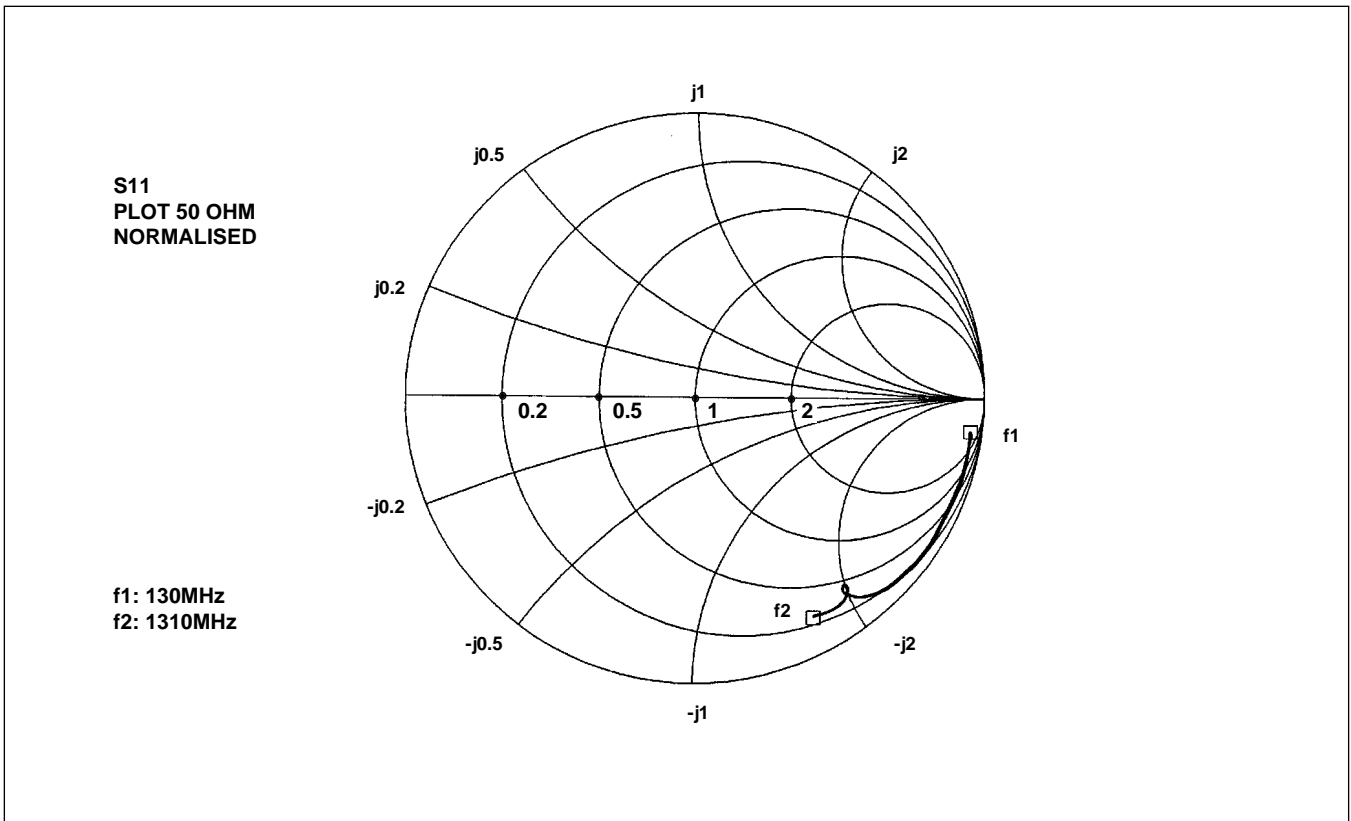


Fig. 6 Typical S11 parameter for pin 1.  $V_{CC} = +5.0V$

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R( )

jx( )

*Fig. 7 Typical input impedance v. frequency*

FREQ-MHZ	R ( )	jx ( )
130.000	255.068	-733.538
153.600	153.362	-688.623
177.200	153.330	-583.339
200.800	115.187	-545.839
224.400	88.649	-482.377
248.000	80.815	-441.798
271.600	71.050	-411.502
295.200	56.207	-369.645
318.800	39.526	-346.620
342.400	41.338	-323.129
366.000	38.779	-304.804
389.600	39.210	-280.556
413.200	23.809	-269.674
436.800	21.221	-255.279
460.400	27.545	-245.161
484.000	23.333	-234.680
507.600	22.227	-224.572
531.200	19.931	-211.375
554.800	17.767	-203.241
578.400	17.636	-194.613
602.000	14.607	-186.545
625.600	12.479	-182.049
649.200	13.075	-174.839
672.800	12.891	-168.320
696.400	12.583	-160.468
720.000	11.250	-156.267
743.600	10.213	-149.642
767.200	10.187	-145.328
790.800	11.269	-143.144
814.400	11.081	-137.557
838.000	10.509	-132.750
861.600	10.063	-129.254
885.200	10.172	-124.495
908.800	10.745	-120.568
932.400	10.841	-118.100
956.000	10.884	-113.395
979.600	12.260	-109.552
1003.20	12.984	-105.975
1026.80	14.508	-103.110
1050.40	16.625	-99.886
1074.00	19.260	-98.149
1097.60	22.799	-98.605
1121.20	23.285	-99.907
1144.80	21.149	-100.925
1168.40	18.956	-99.639
1192.00	16.434	-98.425
1215.60	14.377	-95.033
1239.20	13.743	-92.553
1262.80	12.711	-89.249
1286.40	12.776	-86.081
1310.00	12.598	-82.581

Table.2 Coefficients for Fig.7

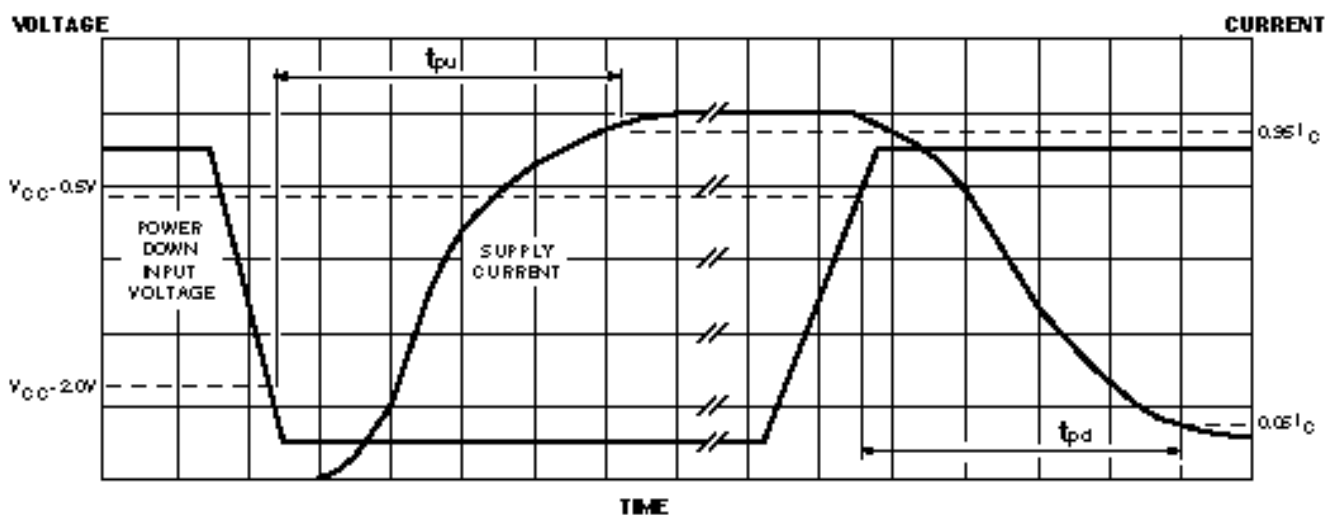


Fig. 8 Power up and power down

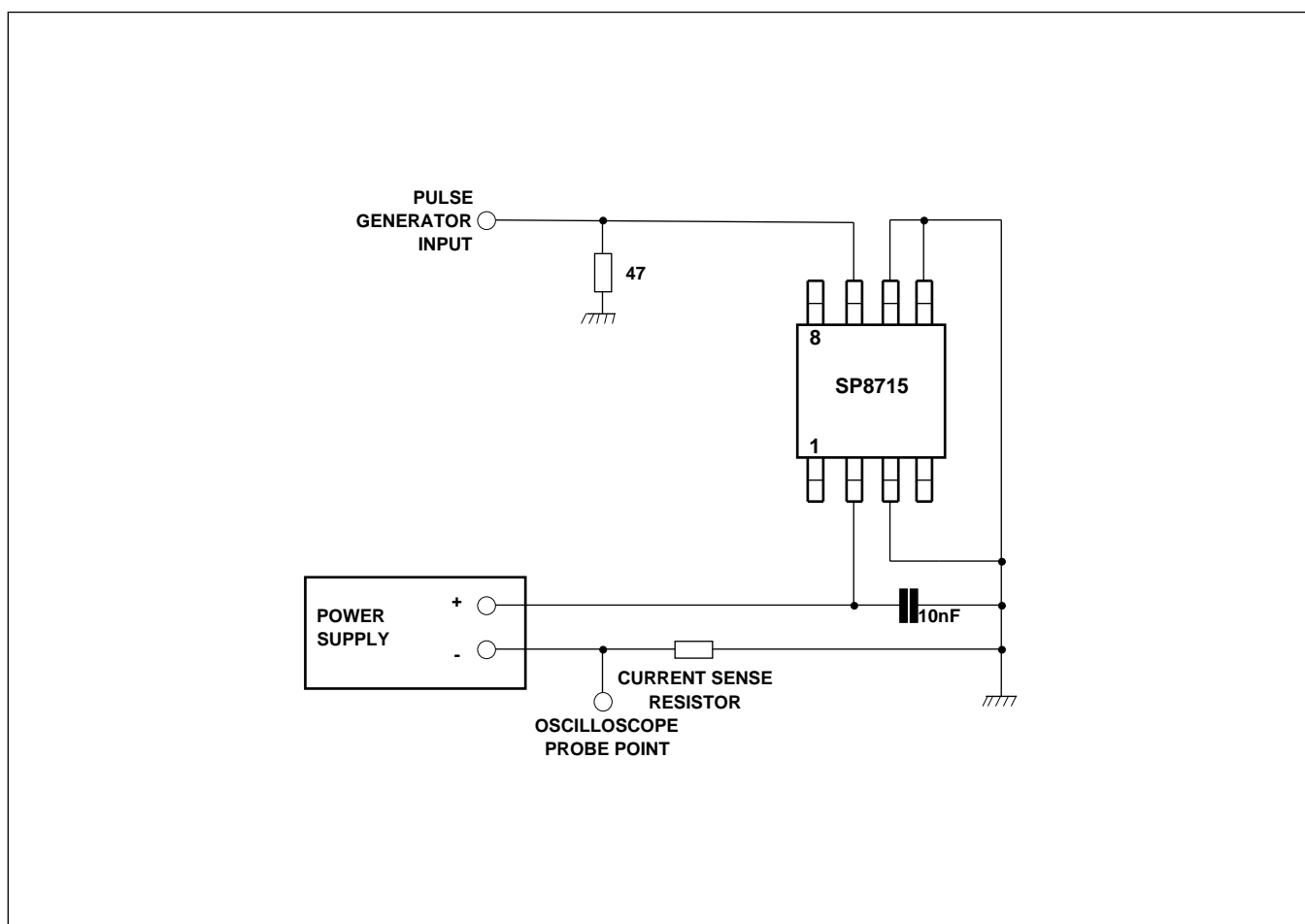


Fig. 9 Power-down time test circuit



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